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Question Paper Code : 11290

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2026.

Fourth Semester

Electrical and Electronics Engineering

EE3402 — LINEAR INTEGRATED CIRCUITS

(Regulations 2021)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Define the term Oxidation in IC fabrication process.
2. List out the types of IC resistor fabrication.
3. Define Input Bias current in op-amp.
4. What is an I to V converter?
5. Define cut-off frequency in Active filter.
6. Define resolution in DAC.
7. What is meant by phase error in PLL?
8. Why 555 Timer is called a versatile IC?
9. What is a linear voltage regulator?
10. Define load regulation.

PART B — ($5 \times 13 = 65$ marks)

11. (a) Describe the different IC fabrication process with neat sketch.

Or

- (b) Discuss the different types of IC Capacitor fabrication with neat sketch.

12. (a) Explain the Adder - Subtractor combinational circuit with neat sketch.

Or

- (b) Explain the operation of Integrator and Differentiator circuit with neat sketch and also draw the outputs of this Integrator and Differentiator when the inputs are sine and square wave.

13. (a) Explain the working of a Negative clamper circuit and also draw the output when the inputs are

(i) $V_i = 50 \sin \omega t$ and $V_{ref} = +10V$

(ii) $V_i = 50 \sin \omega t$ and $V_{ref} = -10V$.

Or

- (b) Explain the operation of R-2R Ladder DAC with neat sketch.

14. (a) Describe the operation of a Monostable multivibrator using 555 timer with neat sketch.

Or

- (b) Describe the operation of vCO and phase detector in PLL.

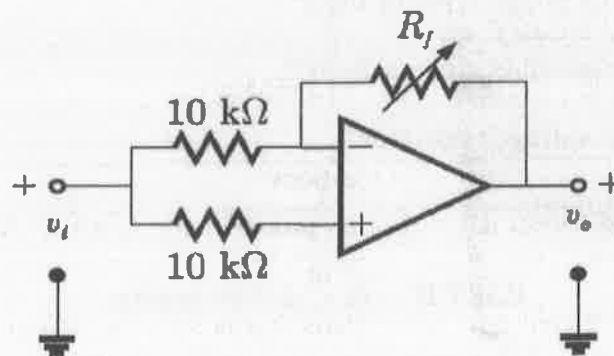
15. (a) Discuss the working of LM317 IC voltage regulator.

Or

- (b) Discuss the operation of SMPS with neat sketch.

PART C — (1 × 15 = 15 marks)

16. (a) In the ideal op-amp circuit given in the adjoining figure, the value of R_f varied from $1 \text{ k}\Omega$ to $100 \text{ k}\Omega$. Find the gain.



Or

(b) Assuming that the Op-amp in the circuit shown is ideal, Find V_o .

